CLAIMS

I claim:

1. A processor that is configured to execute program instructions that are stored in a memory, comprising

a default-register that is configured to contain a default-destination-address, and

wherein

the program instructions include:

a first instruction that is configured to cause the processor to load a specified address into the default-register to form the default-destination-address, and

a second instruction that is configured to cause the processor to subsequently execute program instructions that are located in the memory at the default-destination-address contained in the default-register.

2. The processor of claim 1, wherein

the second instruction includes a condition test and is further configured to cause the processor to execute program instructions that are located at the default-destination-address in dependence upon a result of the condition test.

3. The processor of claim 1, wherein

the default-register is further configured to contain a default-condition-test, and

wherein

the second instruction is further configured to cause the

processor to execute program instructions that are located at the default-destination-address in dependence upon a result of the default-condition-test contained in the default-register.

4. The processor of claim 1, wherein

the second instruction is further configured to cause the processor to execute program instructions that are located at the default-destination-address in dependence upon a result of a prior condition-test.

5. The processor of claim 1, wherein

the default-register is further configured to contain a default-condition-test, and

wherein

the program instructions further include:

a third instruction that is configured to cause the processor to execute program instructions that are located at another specified address in dependence upon a result of the default-condition-test contained in the default-register.

Cont A1

6. A processor that is configured to execute program instructions that are stored in a memory, comprising

a default-register that is configured to contain a default-condition-test, and

wherein

the program instructions include:

a first instruction that is configured to cause the processor to load a specified condition into the default-register to form the default-condition-test, and

a second instruction that is configured to cause the processor to subsequently execute program instructions that are located in the memory at a destination-address, based on a result of the default-condition-test.

Cont A1

7. A method of controlling a sequence of program instructions comprising:

executing a first instruction that specifies a destination-address,

executing a second instruction that causes the destination-address to become a next instruction address, and

executing a third instruction that is located at the next instruction address.

8. The method of claim 7, further including

executing a fourth instruction, before executing the second instruction, that specifies a condition-test, and

wherein

causing the destination-address to become the next instruction address is dependent upon a result of the condition-test when the second instruction is executed.

9. The method of claim 7, further including

saving a result of a condition-test, before executing the second instruction, and

wherein

causing the destination-address to become the next instruction address when executing the second instruction is dependent upon the result of the condition-test.

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